400G PAM4 QSFP-DD DR4/DR4+ Transceiver

FEATURES

- Compliant with IEEE 400GBASE-DR4 optical interface standard and 4x 100GBASE-FR1 optical interface specification for use in 400G or 4x100G breakout applications up to 2 km
- Electrical interface compliant with IEEE 802.3bs 400GAUI-8 (CDAUI-8) standard
- Compact Type 2 QSFP-DD form-factor for high faceplate density in networking equipment and cage backward compatibility with QSFP28
- Compatibility with single-mode optical connectors and cable infrastructures
- Operating temperature range: 0° to 70°C
- CMIS-compliant management interface with full module diagnostics and control through I2C
- Single 3.3V Power supply
- Power consumption<12 W
- RoHS-6 Compliance

APPLICATIONS

- 400GbE connectivity or 4x100GbE breakout connectivity for

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	TCASE	0	30	70	°C
	V_{CC}	3.135	3.3	3.465	V
		-	-	50	mVpp

Optical Transmitter

The 400G DR4+ optical transceiver electrical interface is compliant to the IEEE 802.3bs 400GAUI-8 (CDAUI-8) host to module retimed interface (see IEEE 802.3bs Annex 120E). The 400G DR4+ optical transmitter is compliant with the IEEE 802.3bs 100GBASE-FR1 specification, with four channels of 100G PAM4 data on parallel single-mode fiber (100G per fiber), with an optical reach of up to 2km. Each optical lane is compliant with the 100G Lambda MSA 100G-FR optical interface specification. The DR4+ optical interface standard is defined assuming IEEE standard 400G KP4 RS (544,514) forward error correction (FEC) implemented in the host or switch equipment in order to enable error-free link operation.

TRANSMITTER ELECTRICAL CHARACTERISTICS

TRANSMITTER OPTICAL CHARACTERISTICS

TRANSMITTER OPTICAL CHARACTERISTICS CONT.

400G DR4 (500M PRODUCT VARIANT)						
	Pave	-2.9	-	4	dBm	
	OMA_{outer}	-0.8	-	4.2	dBm	
	TDECQ	-	-	3.4	dB	
		- 2.2	-	-	dBm	
	ER	3.5	-	-	dB	
	Tx_t	-	-	17	ps	
		-	-	-30	dBm	
		-	-	-26	dB	1
	RIN	-	-	-136	dB/Hz	
	ORLT	-	-	21.4	dB	
		2	-	500	m	

(1) Transmitter reflectance is defined looking into the transmitter

Optical Receiver

The 400G DR4 optical transceiver electrical interface is compliant to the IEEE 802.3bs 400GAUI-8 (CDAUI-8) host to module retimed interface (see IEEE 802.3bs Annex 120E). The 400G-DR4+ optical receiver is compliant with the IEEE 802.3bs 100GBASE-FR1 standard with additional support for each optical lane being compliant with the 100G Lambda MSA 100G-FR optical interface specification. The DR4+ optical interface is defined assuming IEEE standard 400G KP4 RS(544,514) forward error correction (FEC) implemented in the host or switch equipment in order to enable error-free link operation

RECEIVER ELECTRICAL CHARACTERISTICS

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS

1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply, Receiver	2B	2
11	LVCMOS-I/O	SCL	2 Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2 Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

QSFP-DD MODULE ELECTRICAL CONNECTOR PIN DEFINITIONS CONT.

73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	3
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	3
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and power supply. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Receiver Electrical Characteristics Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Power Supply

Here we describe the power supply filtering requirements and the power supply sequencing requirements.

POWER SUPPLY FILTERING

The power supply filtering requirements for the 400G DR4 QSFP-DD Optical Transceiver have been designed to be consistent with

LOW POWER MODE

	P_lp	-	-	1.5	W
	Icc_ip_lp	-	-	600	mA
	Icc_sp_lp	-	-	495	mA
	Icc_lp	-	-	478	mA

HIGH POWER MODE

	P_6	-	10	12	W
	Icc_ip_6	-	-	4800	mA
	Icc_sp_6	-	-	3960	mA
	Icc_6	-	-	3636	mA

POWER SUPPLY SEQUENCING

Control and Monitoring Interface

The optical transceiver supports a full QSFP-DD-compliant set of control, alarm, and monitoring features through a standard I^2C management interface, as well as low speed control pins which support additional module control and interrupt features.

LOW SPEED ELECTRICAL HARDWARE INTERFACE

In addition to the I^2C interface, the optical transceiver also supports low speed control pins which provide immediate easy access to key module functions and provide additional user interface signals to support the management interface.

ResetL

ResetL (LVTTL-I signal) is an input pin. The ResetL pin has a weak pull-up in the module to Vcc. A low level on the ResetL pin for longer than the minimum pulse length (t_reset_init > 2µs) initiates a complete module reset and returns all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the “Low” level signal on the ResetL pin is released.

ModPrsL

ModPrsL (LVTTL-O signal) is pulled up to Vcc on the host board and grounded in the module. The ModPrsL pin is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL

IntL (LVTTL-O signal) is an output signal. When IntL is asserted “Low”, it indicates a possible module operational fault, LOS condition or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

ModSelL

The ModSelL (LVTTL-I signal) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands, otherwise it does not. The ModSelL signal has a weak pull-up in the module connected to Vcc.

InitMode

InitMode (LVTTL-I signal) is an input signal. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until host software enables the transition to High Power Mode, as outlined in the Management Interface description below. Under hardware control, the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. The InitMode signal has a weak pull-up in the module connected to Vcc.

SCL

The SCL pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface clock for the module. The SCL signal requires a pull-up resistor on the host board; ≤ 3 kΩ is recommended. Note that SCL and SDA timing specifications are defined in section defined in “Management Interface Timing.”

SDA

The SDA pin (LVCMOS-I/O open-drain signal) is the 2-wire serial interface data for the module. The SDA signal requires a pull-up resistor on the host board; ≤ 3 kΩ is recommended. Note that SCL and SDA timing specifications are defined in section defined in “Management Interface Timing.”

Management Interface

GENERAL FUNCTIONALITY

An I^2C interface shall be used for management interface between the optical transceiver and the host system. The communication protocol shall follow the industry standard QSFP-DD management interface specification. Additional detail and clarified functionality is described in this sub-section.

MODULE STATE MACHINES

The module behavior during power-up, mode changes, and TlcE M212(c

MODULE STATES BEHAVIOR

Reset	Low power	Reset signal deasserted	Suppress all	DataPathDeactivated
MgmtInit	Low power	Module management interface ready AND interrupt signal asserted OR 2s timeout	Suppress all	DataPathDeactivated
ModuleLowPwr	Low power	Host requests an action that requires high power mode	All module flags permitted	DataPathDeactivated
ModulePwrUp	High power	Power up activities are compl (e c)wer up activities are h0 Td[(r)-30.1 (m (c)-/n1)-6.95)-121 (h)-ta6 (		
)-11.1 (h)-7.7 (p)-16.5 (o)-1.8 (we)-15.9 (r)]TJ0.02 Tc 0 Tw 8.96 0 TdTd[H)-7.7 (o)-3 (s)-4.1 (t r)4.4 (e)-11.7 (q)-0.8 (u)-8 (e)-3.6 (s)-4.2 (t)-0.7 (s a)-7 (o)-8.1				
35tMID iutLow power				

DATA PATH STATE BEHAVIOR

DataPathDeactivated	Quiescent	Quiescent	Suppress all data path flags	Host sets DataPathPwrUp bit(s)
DataPathInit	Quiescent	Quiescent	Suppress all	Module completes data path power up and initialization
DataPathActivated	See Byte 54h	Active	All data path flags permitted	1) Host clears DataPathPwrUp bit(s) AND module is active 2) Host requests data path reconfiguration
DataPathDeinit	Quiescent	Quiescent	Suppress all	Data path decommissioning complete

MANAGEMENT INTERFACE (I^2C) TIMING

Timing and other specs for the I^2C communication/management interface are given in the table below.

Label Specification

The following printed label is attached to the product (note that the certification labels will be added/removed according to requests and certification process results):

Regulatory and Compliance

	• EN 55024 (EU) • IEC EN 61000-4-3 (International)	• EMC Directive 89/336/EEC • IEC /CISPR/24
	• CISPR 22, class B (Comité International Spécial des Perturbations Radioélectriques--CISPR; Special international committee on radio interference. International). • AS/NZS CISPR22 (Australia/New Zealand)	• VCCI-03 (Japan) • FCC 47 CFR Part 15, class B (US) • ICES-003, Issue 4 (Canada) • EN 55022 (EU) • EMC Directive 2004/108/EEC (EU)
	•r Tw (l)-1.5 (a)106 -31.3 (4028 Tc -0r(N)-59)-7.N7.7 (/)S5.3 (e I3.3 (s /T1 1 Tf(0)-16.7 (0-19.2 -2. (s N)-4-2.5 (C54	